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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,039	03/06/2001	Pervez Hassan Sagarwala	93-C-091C1 (STMI01-00012)	7946

30425 7590 06/19/2002

STMICROELECTRONICS, INC.
MAIL STATION 2346
1310 ELECTRONICS DRIVE
CARROLLTON, TX 75006

EXAMINER	
PRENTY, MARK V	
ART UNIT	PAPER NUMBER
2822	4

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/800,039	Applicant(s) SAGARWALA et al.
	Examiner Prenty	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Mar 6, 2001* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-7 and 27-39* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-7 and 27-39* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *3*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

This Office Action is in response to the papers filed March 6, 2001.

Claims 1-7 and 28-39 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Independent claim 1 is indefinite because "a minimum channel length required for the p-channel transistors" and "a minimum channel length for the respective p-channel transistor," are indefinite.

Claims 2-7 depend on independent claim 1 and are thus similarly indefinite.

Dependent claim 5 is further indefinite because "a distance below which the transistor will not operate reliably due to short channel effects," and "a distance above which the transistor will not turn on efficiently," are indefinite.

Dependent claim 6 is further indefinite because "a distance below which the transistor will not operate reliably due to short channel effects," and "a distance above which the transistor will not turn on efficiently," are indefinite.

Claim 28 is indefinite because "the minimum channel length required for the p-channel transistor" is indefinite.

Claims 29-32 depend on claim 28 and are thus similarly indefinite.

Claim 29 is further indefinite because "the minimum channel length required for the p-channel transistor" is indefinite.

Claims 30-32 depend on claim 29 and are thus similarly indefinite.

Claim 30 is further indefinite because "the minimum channel length required for the p-channel transistor" and "a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor," are indefinite.

Claim 32 is further indefinite because "a minimum channel length required for

the n-channel transistor" is indefinite.

Independent claim 33 is indefinite because "a minimum channel length required for the p-channel transistor" is indefinite.

Claims 34-39 depend on independent claim 33 and are thus similarly indefinite.

Claim 35 is further indefinite because "the minimum channel length required for the p-channel transistor" and "a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistor," are indefinite.

Claims 36 and 37 depend on claim 35 and are thus similarly indefinite.

Claims 27, 28, 33 and 34, at least insofar as understood, are rejected under 35 U.S.C. §102(b) as being anticipated by Miyajima et al. (United States Patent 5,273,914 submitted in the Information Disclosure Statement filed May 24, 2001).

With respect to independent claim 27, Miyajima et al. disclose a CMOS integrated circuit structure (see Fig. 13(h)), comprising: an n-channel transistor including lightly doped source and drain regions 8 within a p-type region 2 of a substrate 1; and a p-channel transistor without lightly doped source and drain regions within an n-type region 3 of the substrate, the p-channel transistor including: a gate electrode 6 having a width less than a channel length of a channel for the p-channel transistor; and first sidewall spacers 9 adjacent opposing sides of the gate electrode 6 and overlying at least a portion of the channel for the p-channel transistor.

Claim 27 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Miyajima et al.

With respect to dependent claim 28, the width of Miyajima et al's gate electrode 6 is less than "the minimum channel length required for the p-channel transistor."

Claim 28 is thus rejected under 35 U.S.C. §102(b) as being anticipated by

Miyajima et al.

With respect to independent claim 33, Miyajima et al. disclose an intermediate structure for use in forming a CMOS integrated circuit (see Fig. 13(g)), comprising: a p-type region 2 for an n-channel transistor including lightly doped source and drain regions 8; an n-type region 3 for a p-channel transistor without lightly doped source and drain regions; a gate electrode 6 overlying a portion of the n-type region, the gate electrode having a width less than "a minimum channel length required for the p-channel transistor"; and an insulating layer 22 over a top and sides of the gate electrode 6, the insulating layer having a thickness which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds "the minimum channel length required for the p-channel transistor."

Claim 33 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Miyajima et al.

With respect to dependent claim 34, Miyajima et al's insulating layer 22 forms a mask for implanting source and drain regions for the p-channel transistor.

Claim 34 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Miyajima et al.

Claims 27-30 and 32, at least insofar as understood, are rejected under 35 U.S.C. §102(e) as being anticipated by Chen (United States Patent 5,766,991 submitted in the Information Disclosure Statement filed May 24, 2001).

With respect to independent claim 27, Chen discloses a CMOS integrated circuit structure (see Fig. 13), comprising: an n-channel transistor including lightly doped source and drain regions within a p-type region 10 of a substrate 14; and a p-channel transistor without lightly doped source and drain regions within an n-type

region 12 of the substrate, the p-channel transistor including: a gate electrode having a width less than a channel length of a channel for the p-channel transistor; and first sidewall spacers adjacent opposing sides of the gate electrode and overlying at least a portion of the channel for the p-channel transistor.

Claim 27 is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to dependent claim 28, the width of Chen's gate electrode is less than "the minimum channel length required for the p-channel transistor."

Claim 28 is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to dependent claim 29, Chen's first sidewall spacers have a width which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds "the minimum channel length required for the p-channel transistor."

Claim 29 is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to dependent claim 30, Chen's first sidewall spacers have a width which, taken on opposing sides of the gate electrode and combined with the width of the gate electrode, exceeds "the minimum channel length required for the p-channel transistor" plus "a diffusion distance for implanted dopants forming source and drain regions for the p-channel transistors."

Claim 30 is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

With respect to dependent claim 32, Chen's n-channel transistor further

comprises: a gate electrode having a width approximately equal to a "minimum channel length required for the n-channel transistor"; and sidewall spacers adjacent to opposing sides of the n-channel transistor gate electrode and overlying the lightly doped source and drain regions.

Claim 32 is thus rejected under 35 U.S.C. §102(e) as being anticipated by Chen.

Sagarwala (United States Patent 6,221,709) is related to this application.

Registered practitioners can telephone the examiner at (703) 308-4939. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the application's Serial Number.

Technology Center 2800's general telephone number is (703) 308-0956.

Mark Prenty

Mark V. Prenty
Primary Examiner